



(43) International Publication Date
17 March 2005 (17.03.2005)

PCT

(10) International Publication Number
WO 2005/024624 A1

(51) International Patent Classification⁷: G06F 5/06,
H04J 3/06

(21) International Application Number:
PCT/EP2004/009394

(22) International Filing Date: 23 August 2004 (23.08.2004)

(25) Filing Language: English

(26) **Publication Language:** English

(30) Priority Data:
103 42 255.2 11 September 2003 (11.09.2003) DE

(71) Applicant (for all designated States except US): THOMSON LICENSING S.A. [FR/FR]; 46, Quai Alphonse le Gallo, F-92100 Boulogne Billancourt (FR).

(72) Inventor; and

(75) **Inventor/Applicant (for US only):** LOEW, Andreas
[DE/DE]; Neckarring 67, 64521 Gross-Gerau (DE).

(74) **Agent:** ROSSMANITH, Manfred; Deutsche Thomson-Brandt GmbH, European Patent Operations, Karl-Wiechert-Allee 74, 30625 Hannover (DE).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

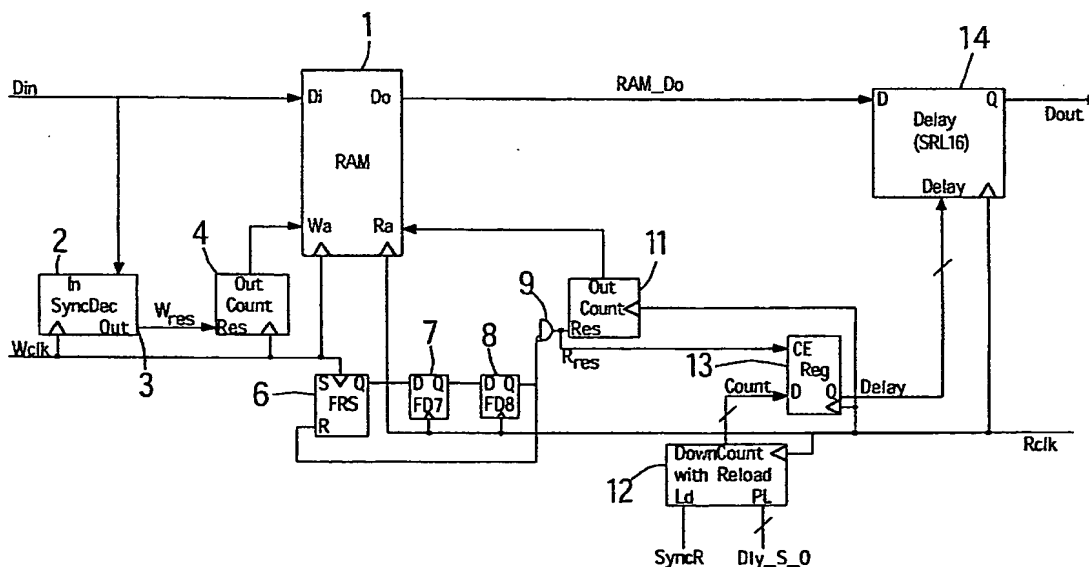
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CIRCUIT FOR ADDRESSING A MEMORY



(57) Abstract: A circuit is proposed which has a memory to which input data can be written at different write addresses with a first clock rate and from which output data can be read at different read addresses with a second clock rate. The memory can be fed a write reset pulse that resets the write address to an initial value. In addition, the memory can be fed a read reset pulse by means of which the data are output in a fixed temporal relationship. Finally, the circuit proposed is provided with switching means in order to derive the read reset pulse from the write reset pulse. This ensures that the two reset pulses cannot occur simultaneously.

WO 2005/024624 A1